ABSTRACT OF THE DISCLOSURE

A semiconductor memory device includes memory cells, redundant cells, a redundancy repair control circuit and a test mode control circuit. Each of the memory cells is assigned a unique address to be accessed by a corresponding address. The redundant cells are replaceable with the memory cells. The redundancy repair control circuit replaces predetermined memory cells among the memory cells with the redundant cells. The test mode control circuit invalidates an operation of the redundancy repair control circuit and assigns an additional unique address to the redundant cells so that all of the memory cells and the redundant cells are accessible during a test mode.